AMENDMENTS TO THE DRAWINGS:

Please replace figures 7-10 with the attached replacement figures 7-10, which are labeled "Replacement Figures" and include the designation "Prior Art".

REMARKS

Claims 1-11 are pending in the present application. Claims 2-4 and 6-11 and figures 7-10 have been amended to correct typographic errors and/or to clarify the patentable subject matter recited therein. No new matter is added. In view of the above amendatory matter and the following remarks, favorable reconsideration of this case is respectfully requested.

Applicants note with appreciation that the Examiner acknowledges that claims 6, 8, 10, and 11 are directed to allowable subject matter, and would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Figures 7-10 have been amended to include the designation "Prior Art". It is therefore respectfully requested that the objection to the drawings be withdrawn.

Claims 2-6 and 8-11 are objected to because of informalities. Claims 2-4 and 8-11 have been amended essentially in accordance with the Examiner's suggestion, with the exception of claim 3, lines 5 and 7, which instead replaces "a cycle of" with "said cycle of". It is respectfully submitted that the claim amendments respond to the objections raised in the Office Action, and it is therefore respectfully requested that the objections be withdrawn.

Claims 7 and 9 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. Claim 7 has been amended to recite that the phase-locked loop circuit has as input signals a signal resulting from division by a variable frequency divider of an *output* clock signal, as suggested by the Examiner. It is respectfully submitted that amended claim 7 is described in figures 1 and 6B, and therefore it is respectfully requested that the rejection of claims 7 and 9 be withdrawn.

Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' Allegedly Admitted Prior Art (hereinafter AAAPA) in view of United States Patent No. 6,658,074 to Murakami (hereinafter Murakami). Applicants respectfully traverse.

Claim 1 relates to a receiver apparatus for receiving digital data in which stuff data have been inserted by stuffing synchronization. The receiver apparatus of claim 1 includes, *inter alia*, a read clock signal regulator for adjusting a cycle of a read clock signal based on an interval in a prescribed order direction from an address designated by a read unit to an address designated by a write unit.

The Examiner admits that the AAAPA does not teach a read clock signal regulator. (Office Action; page 4, lines 5-6). The Examiner asserts that this features is disclosed in Murakami.

However, there is a significant difference between the present invention of claim 1 and the disclosure of Murakami. The present invention controls a read clock based on the interval from an address designated by the read unit to an address designated by the write unit. In contrast, Murakami apparently controls a read clock based on a stuff rate that is a ratio of stuff data of the inputted digital data. (Murakami; Figure 13, elements 654 and 606) The stuff rate may correspond to a write-in cycle to the memory. Therefore, a read-out cycle follows the write-in cycle by the read-out cycle adjusting according to the stuff rate. As a result, if the stuff rate is not changed, the read-out cycle can correspond with the write-in cycle and the interval from the read address to write address can be kept constant.

However, in Murakami, a predetermined time period is required to measure the stuff rate because of the necessity of sampling a plurality of data and performing the calculations. Therefore, a delay is inherent in the method according to Murakami. In Murakami, if the stuff

rate is changed and the write-in cycle becomes faster, the read-out cycle may become relatively slow compared to the write-in cycle, until the read-out cycle follows the write-in cycle, and the memory may therefore be overflowed. As result, to prevent the overflow of the memory in Murakami, a larger-size memory may need to be provided.

In contrast, the present invention directly obtains both the read address and the write address and controls the read clock based on the intervals between both. Therefore, in the present invention the read clock can be adjusted in real time when the write-in cycle is changed.

Additionally, the underflow of memory must also be prevented in communication networks. In Murakami, if the stuff rate is changed and the write-in cycle becomes slower, the read-out cycle may become relatively fast compared to the write-in cycle until the read-out cycle follows the write-in cycle, and the memory may be underflowed. The present invention prevents the overflow and the underflow of the memory of an appropriate size. Since Murakami does not disclose or suggest a read clock signal generator as recited in claim 1, the combination of the references does not render claim 1 unpatentable.

Claims 2-5 depend from claim 1 and are therefore allowable for at least the same reasons claim 1 is allowable.

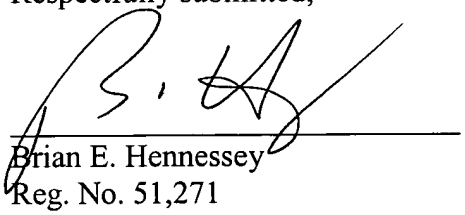
CONCLUSION

In view of the remarks set forth above, this application is believed to be in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully

requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged on Deposit Account 50-1290.

Respectfully submitted,



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